folding said interconnector so that adjacent semiconductor devices are stacked on top of each other.

REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 1-23 were pending in this application. Claims 1, 3, 11, 13, 14, 16, 19, 21, and 22 have been cancelled. Claims 2, 4-10, 12, 15, 17, 18, 20 and 23 have been amended to better define the scope of the claimed invention.

Claims 1-23 stand rejected under 35 U.S.C. 112, second paragraph. The Examiner asserted a lack of clarity in the terms *entry* and *exit* when used in reference to *port*. The claims using those terms have been cancelled. The Examiner also inquired as to how a port may be distinguished from a pad. Applicant replies that *port* is a broader term than *pad*. In other words, a port can be a pad, or it could take a form other than as a pad. In this instance, a port is comparable to a terminal. The term is clear and unambiguous and is used similarly elsewhere in the art of semiconductor devices and packaging. Therefore, Applicant respectfully requests that the rejection be withdrawn.

Claims 1-3, 6-13, and 15-19 stand rejected under 35 U.S.C. 102(e) as being anticipated by Inaba (JP 2001-217388). Claim 15 includes the feature wherein "said interconnector having on said first surface electrically conductive lines for connecting a plurality of packaged semiconductor devices formed on said first surface adjacent to each other" and "at least one additional unpackaged semiconductor device having a plurality of first electrical coupling members, said first coupling members attached to said first plurality ports." Inaba does not

teach or suggest such features. Claims 2, 4-10, and 12 have been amended to depend from Claim 15 and are therefore patentable over Inada for at least the reasons presented above. Claims 1, 3, 11, 13, 16, and 19 have been cancelled.

Claims 4, 14, 20, and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba in view of Denes (U.S. Patent No. 5,220,488). Claims 4 and 14 have been amended to depend from Claim 15. As indicated above Inaba does not teach or suggest all of the features of Claim 15. Denes does not cure the deficiencies of Inaba. Similarly, Claim 23 includes the steps of "forming on said first surface a plurality of packaged semiconductor devices adjacent to each other and connected to said conductive lines; attaching at least one additional unpackaged semiconductor device, having a plurality of first electrical coupling members, to said first plurality ports." Claim 20 has been amended to depend from Claim 23. Therefore, Applicant respectfully submits that Claims 4, 14, and 20 are patentable over Inaba in view of Denes for at least the reasons presented above. Claim 22 has been cancelled.

Claims 5 and 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba. Claims 5 and 8 have been amended to depend from Claim 15. As indicated above, Claim 15 includes features not taught or suggested by Inaba. Therefore, Applicant respectfully submits that Claims 5 and 8 are patentable over Inaba for at least the reasons presented above.

Applicant has submitted an Information Disclosure Statement along with this paper. Newly cited patents 6,121,676 and 6,225,688, while disclosing a folded, stacked structure similar to that of Inaba, do not teach or suggest the abovecited features of Claims 15 and 23. Therefore, Applicant respectfully requests that these references be considered and that the claims pending in this application be passed to issuance.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 2, 4-10, 12, 15, 17, 18, 20 and 23. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend the claims as follows:

1. (cancelled)

2. (amended) The assembly according to Claim 15 [1] wherein said unpackaged semiconductor device is an integrated circuit chip having an active and a passive surface, said first coupling members attached to said active surface.

3. (cancelled)

4. (amended) The assembly according to Claim 15 [1] further comprising at least one passive electrical component integrated into said conductive lines on said interconnector.

5. (amended) The assembly according to Claim 15 [1] wherein said entry ports are spaced apart less than 100 μm center to center, and said exit ports are spaced apart more than 100 μm center to center.

6. (amended) The assembly according to Claim 15 [1] wherein said interconnector is a flexible polyimide film.

7. (amended) The assembly according to Claim 15 [1] wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.

8. (amended) The assembly according to Claim 15 [1] wherein said first and second coupling members are solder balls selected from a group consisting of

pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

9. (amended) The assembly according to Claim 15 [1] wherein said first coupling members are selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy.

10. (amended) The assembly according to Claim 15 [1] further having an adhesive non-conductive polymer underfilling any spaces between said first coupling members attached to said entry ports under said semiconductor device.

11. (cancelled)

12. (amended) The assembly according to Claim 15 [11] further comprising at least one discreet passive electrical component attached to said ports.

13. (cancelled)

14. (cancelled)

15. (amended) A semiconductor assembly comprising:

a strip-like flexible interconnector of electrically insulating material having first and second surfaces;

said interconnector having on said first surface electrically conductive lines for connecting a plurality of packaged semiconductor devices formed on said first surface adjacent to each other;

said interconnect further having electrically conductive paths extending through said interconnector from said first surface to said second surface, forming electrical ports on said second surface;

said ports comprise first and second pluralities, said first plurality ports spaced apart by less, center to center, than said second plurality ports are spaced apart, center to center;

said interconnector folded so that said adjacent semiconductor devices are stacked on top of each other;

at least one additional unpackaged semiconductor device having a plurality of first electrical coupling members, said first coupling members attached to said first plurality ports; and

a plurality of second electrical coupling members attached to said second plurality ports, said coupling members suitable for attachment to other parts.

16. (cancelled)

17. (amended) The method according to Claim 23 [16] further comprising the step of:

integrating at least one passive electrical component into said conductive lines on said interconnector.

18. (amended) The method according to Claim 23 [16] further comprising the step of:

underfilling an adhesive non-conductive polymer into any spaces between said first coupling members attached to said entry ports under said semiconductor device.

19. (cancelled)

20. (amended) The method according to Claim 23 [19] further comprising the step of:

attaching at least one discreet passive electrical component to said ports.

21. (cancelled)

22. (cancelled)

23. (amended) A method of assembling an integrated circuit device, comprising the steps of:

forming electrically conductive lines on a strip-like flexible interconnector of electrically insulating material having first and second surfaces;

forming electrically conductive paths extending through said interconnector from said first surface to said second surface, forming electrical ports on said second surface such that said ports comprise first and second pluralities, said first plurality ports spaced apart less, center to center, than said second plurality ports are spaced apart, center to center;

forming on said first surface a plurality of packaged semiconductor devices adjacent to each other and connected to said conductive lines;

attaching at least one additional unpackaged semiconductor device, having a plurality of first electrical coupling members, to said first plurality ports;

attaching a plurality of second electrical coupling members to said second plurality ports; and

folding said interconnector so that adjacent semiconductor devices are stacked on top of each other.